

[illegible]

A cross-sectional view of a semiconductor device 110. The device is built on a substrate 13. A layer 115 is formed on the substrate. A central region 2 is defined within layer 115, containing a patterned layer 5b and a layer 1b. This central region is flanked by two side regions 5a and 15a. The side regions 5a and 15a are separated by a gap 18. The top surface of the device is covered by a layer 14, which is patterned to form a central region 1a and two side regions 17. The side regions 17 are separated by a gap 16. The device is further defined by a layer 3 at the bottom and a layer 120 at the top.

FIG. 2

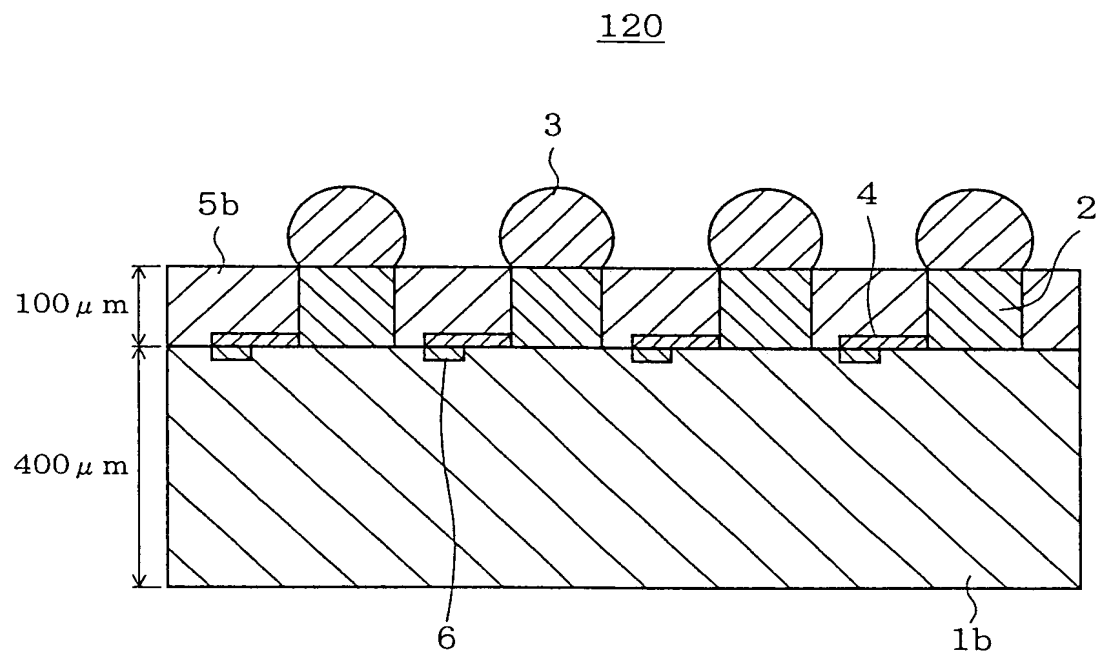


FIG. 3(A)

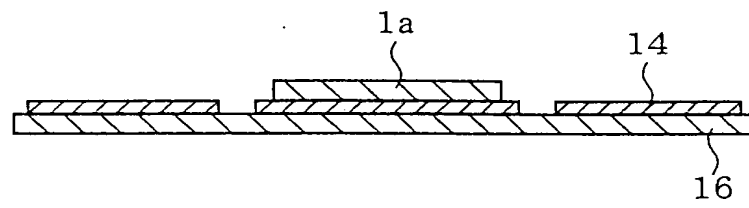


FIG. 3(B)

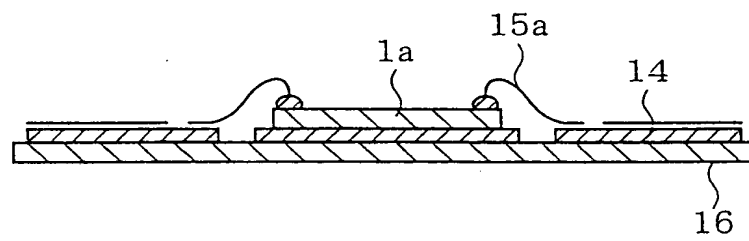


FIG. 3(C)

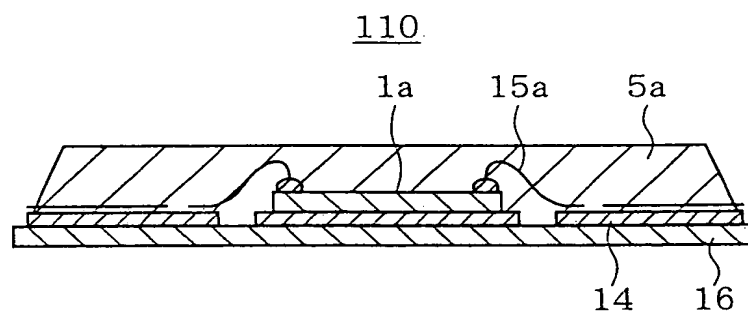


FIG. 4(A)

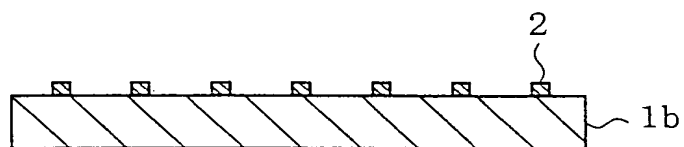


FIG. 4(B)

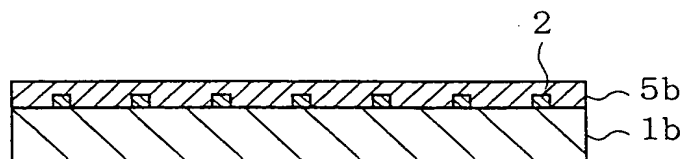


FIG. 4(C)

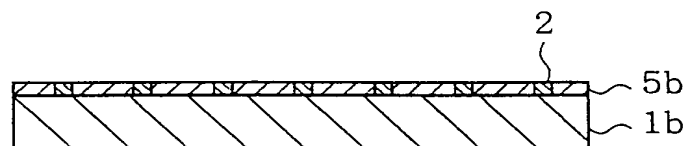


FIG. 4(D)

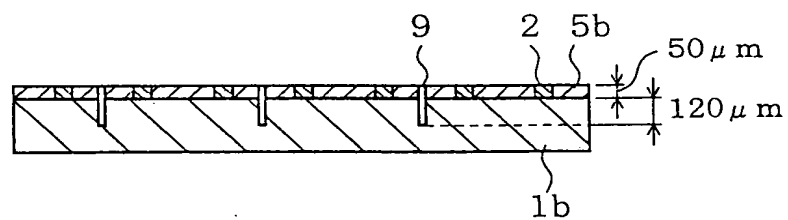


FIG. 4(E)

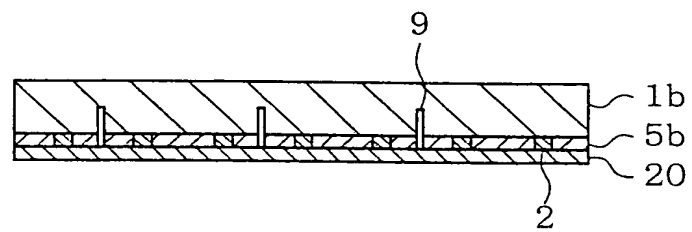


FIG. 4(F)

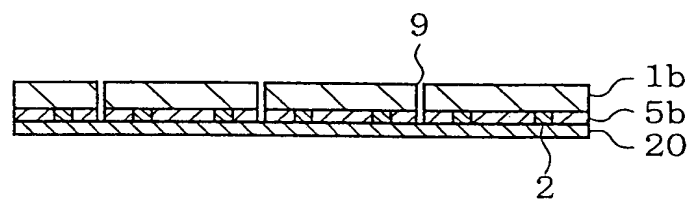


FIG. 4(G)

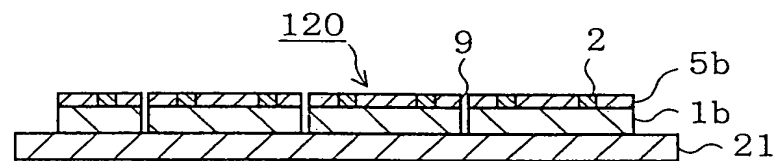




FIG. 5(B)

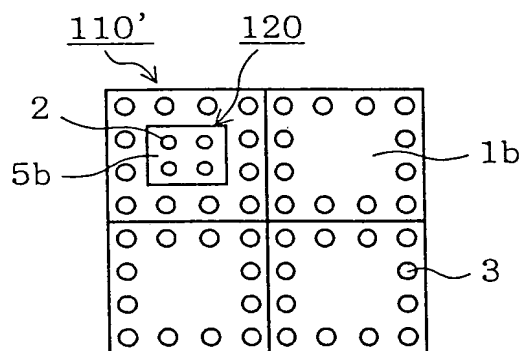


FIG. 6(A)

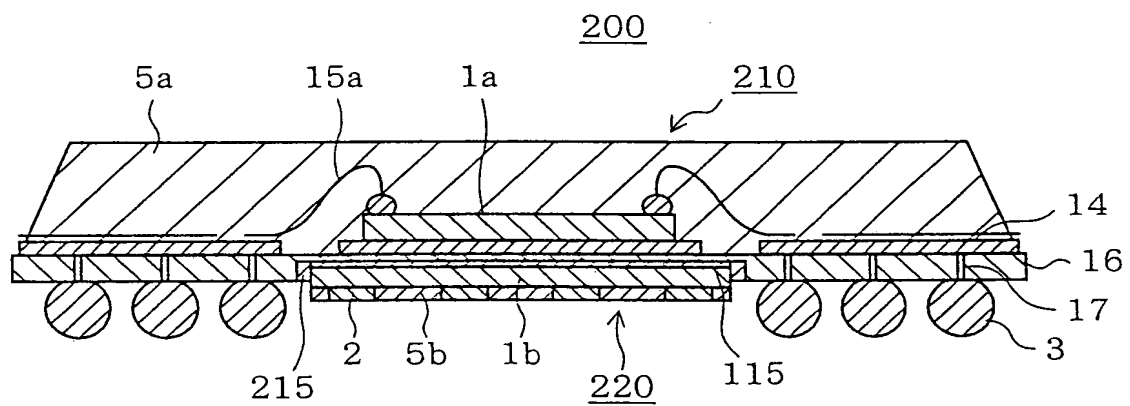


FIG. 6(B)

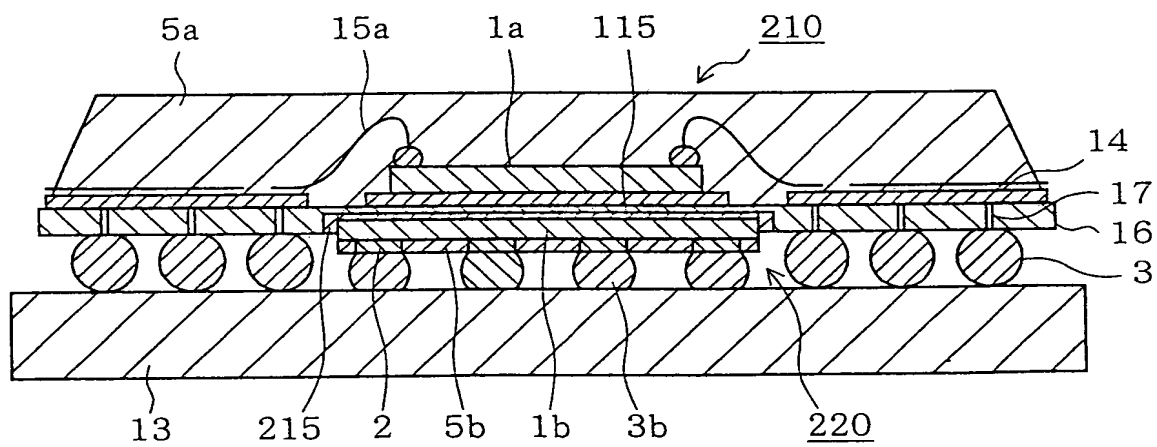




FIG. 7(A)

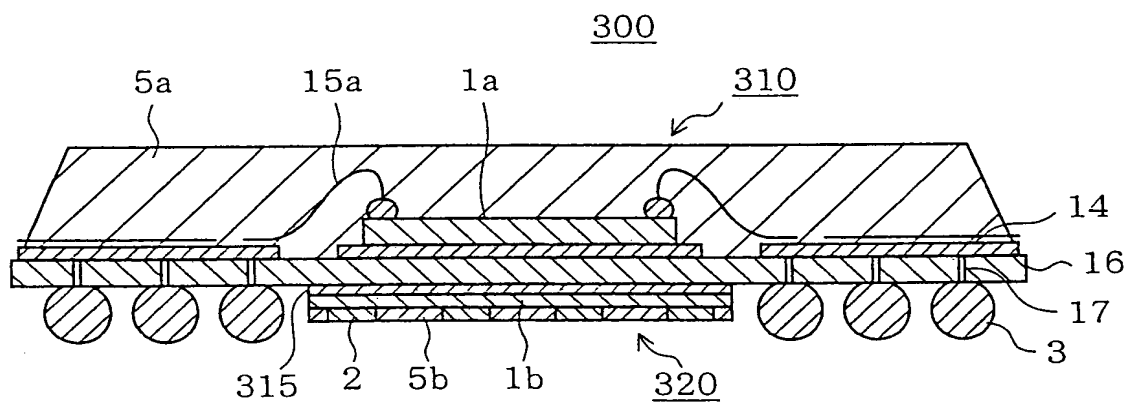


FIG. 7(B)

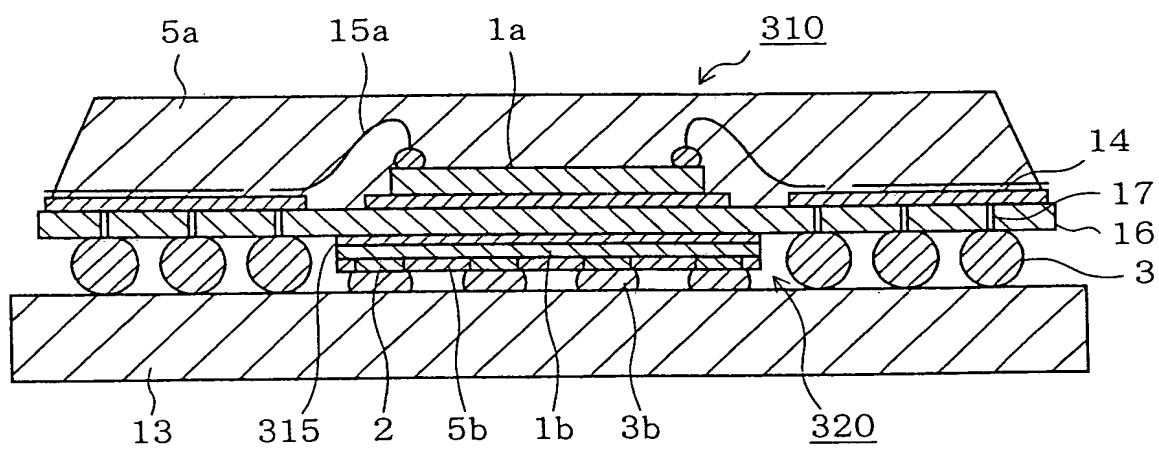


FIG. 8(A)

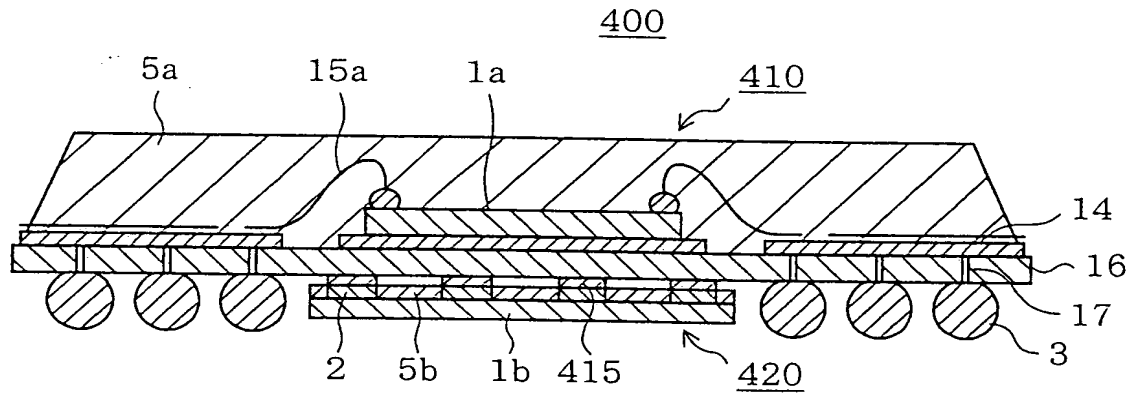


FIG. 8(B)

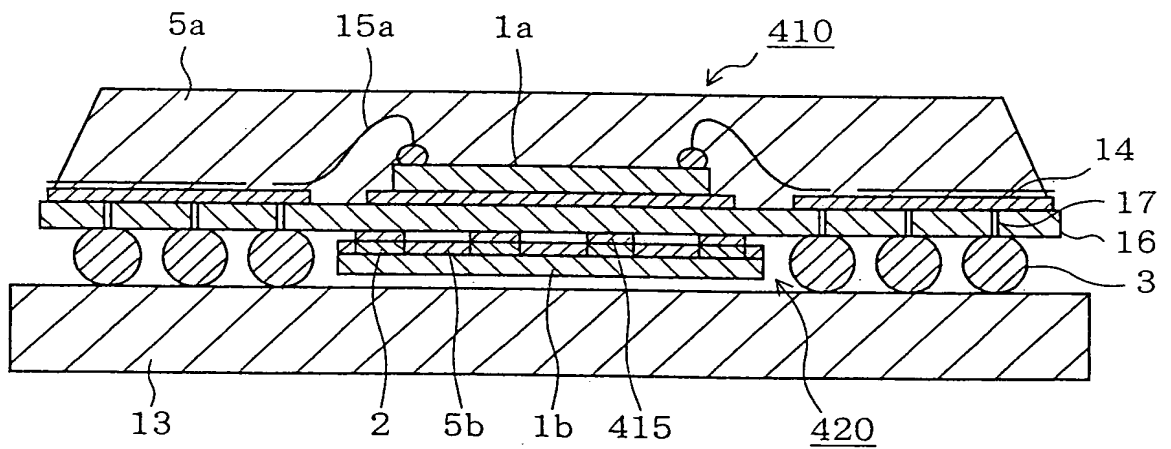


FIG. 9(A)

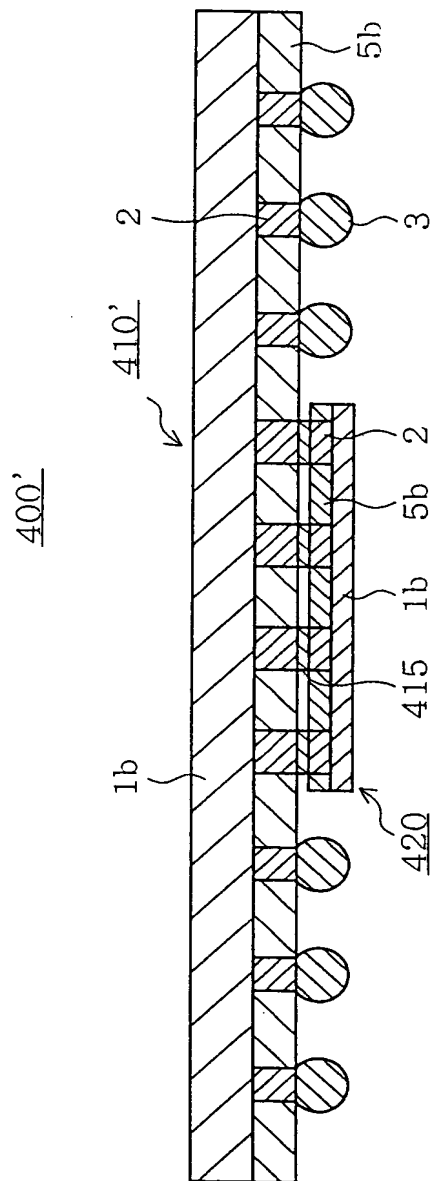


FIG. 9(B)

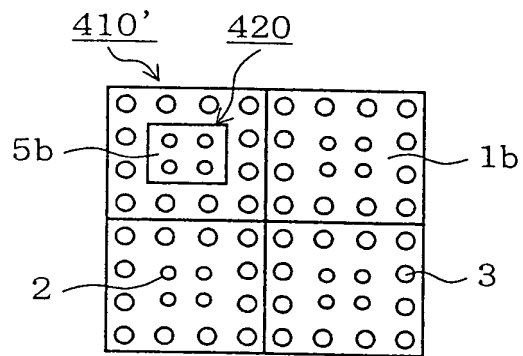


FIG. 10(A)

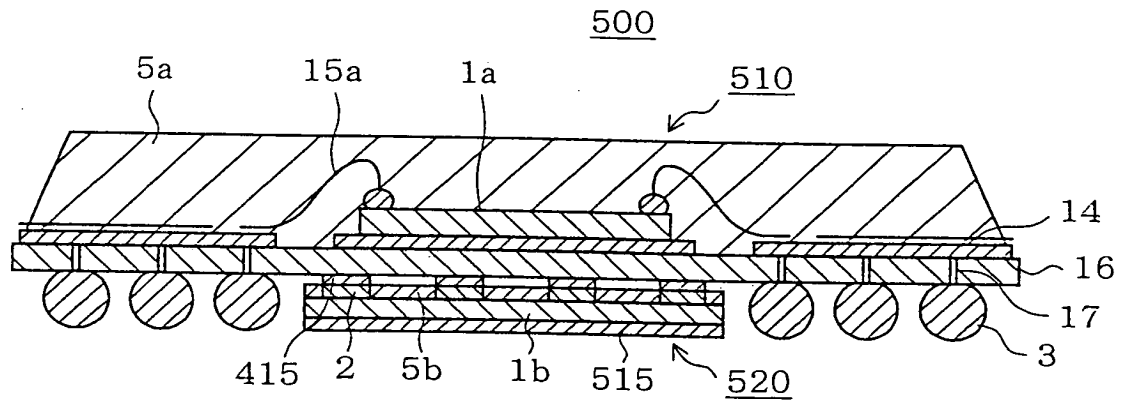


FIG. 10(B)

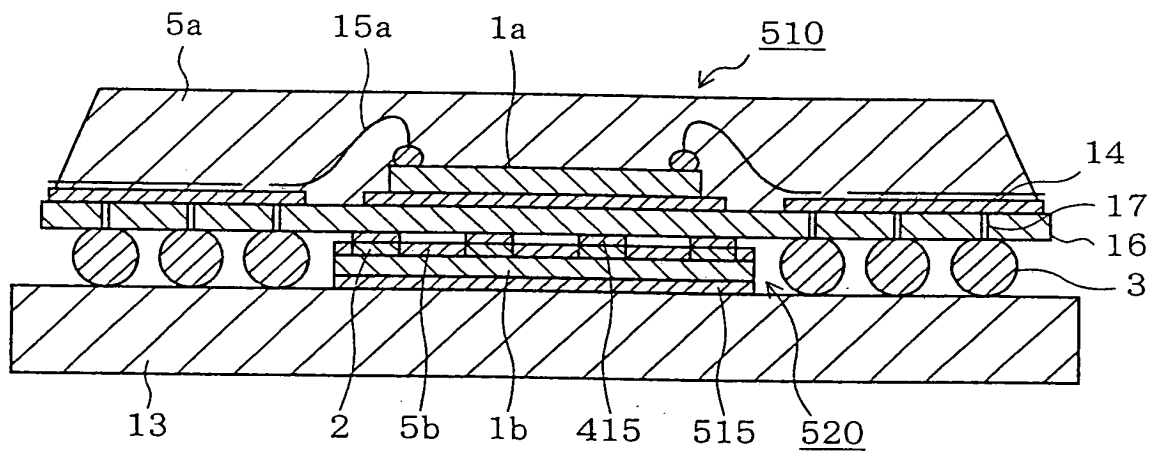


FIG. 11(A)

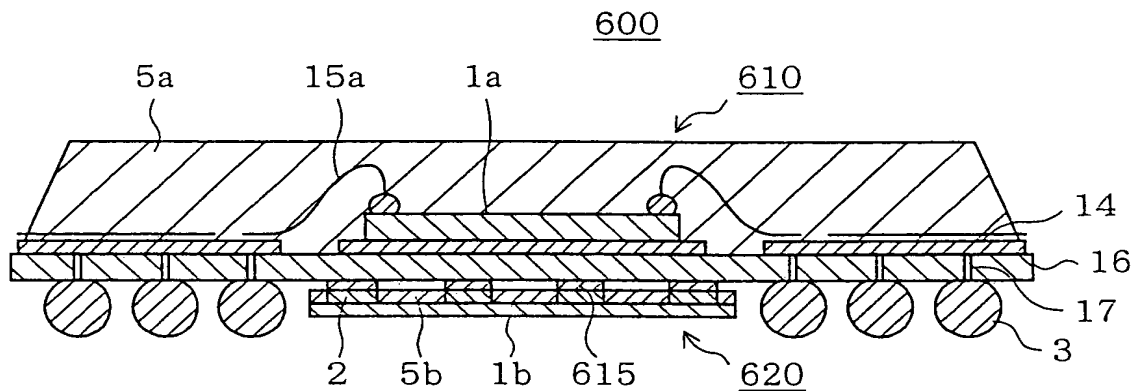


FIG. 11 (B)

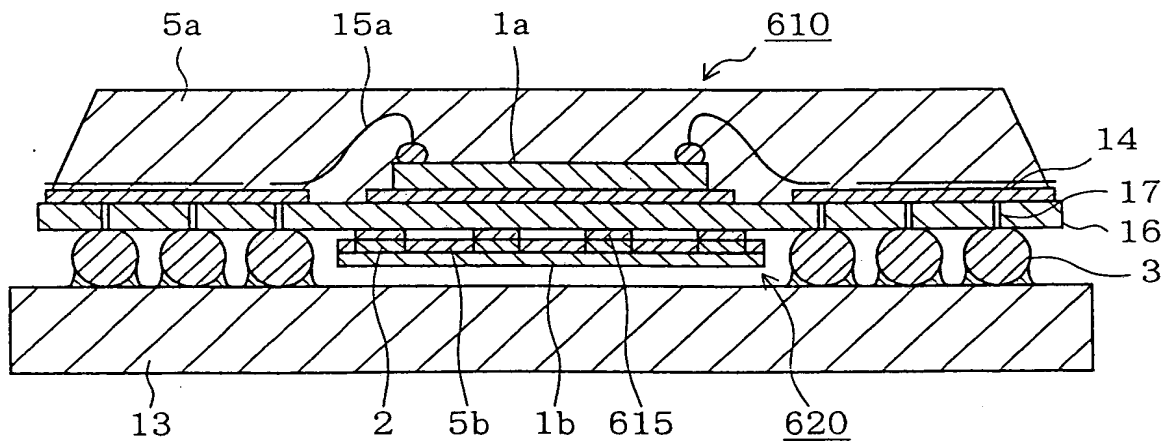


FIG. 12

